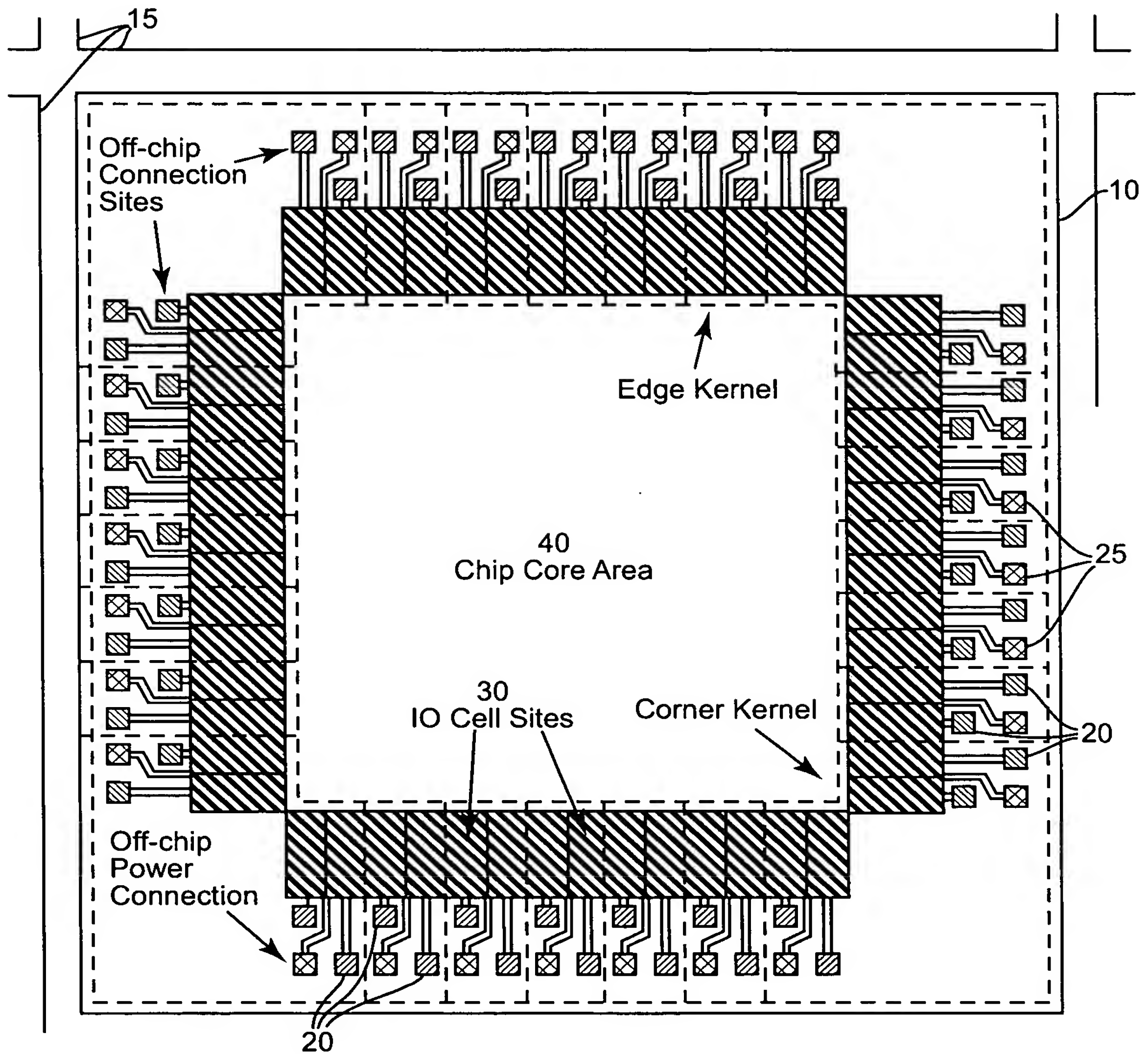
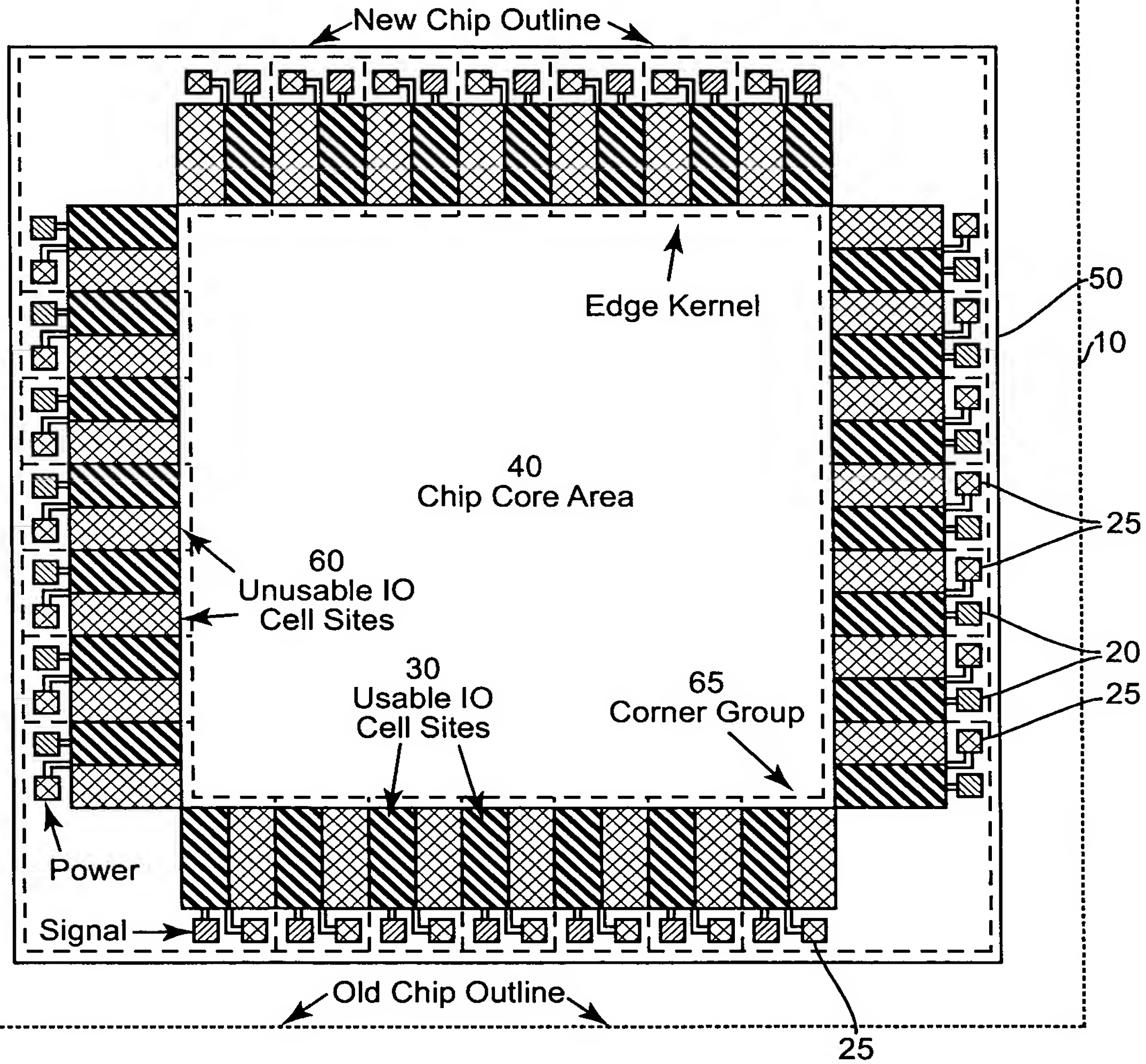




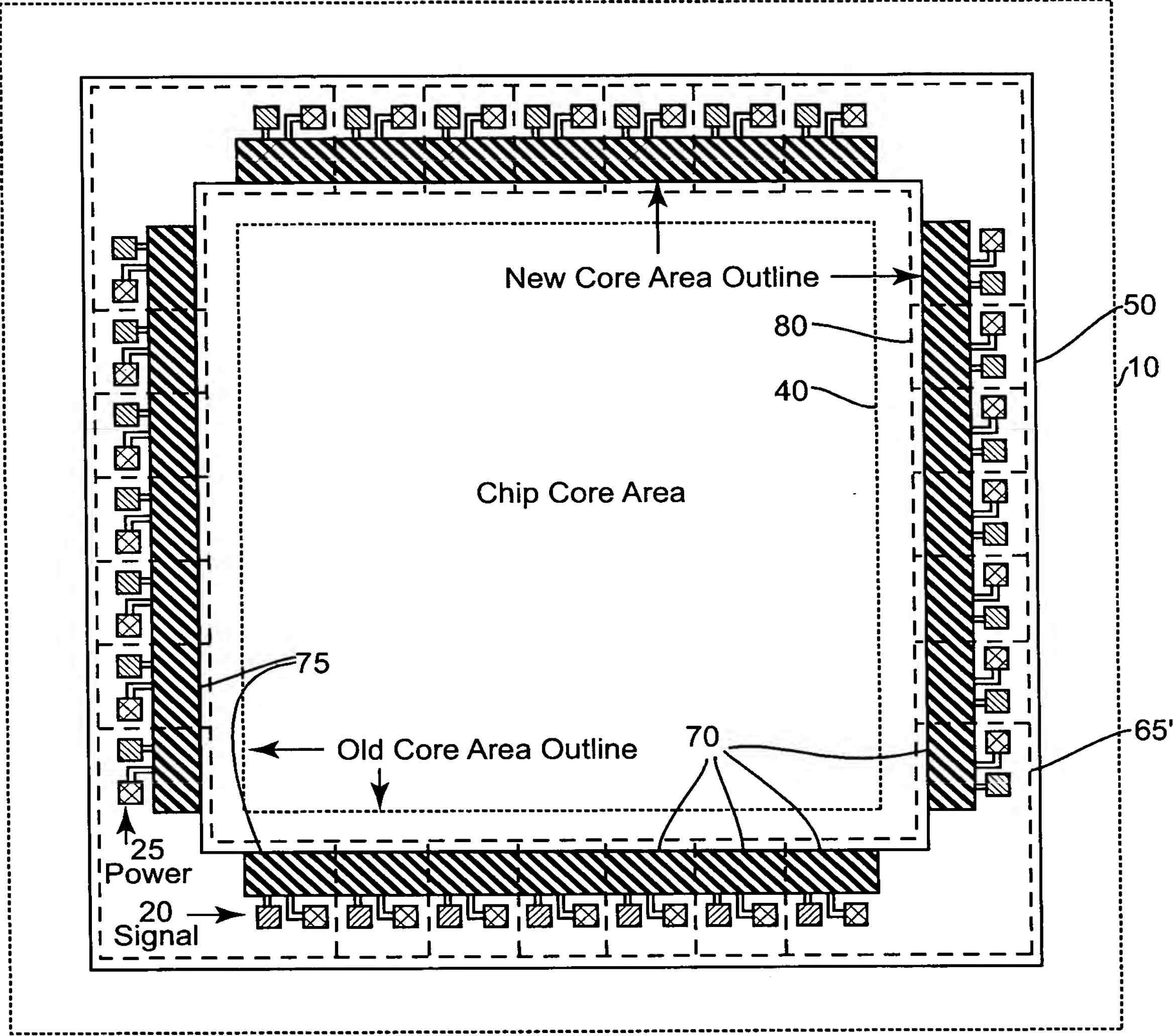
1/11  
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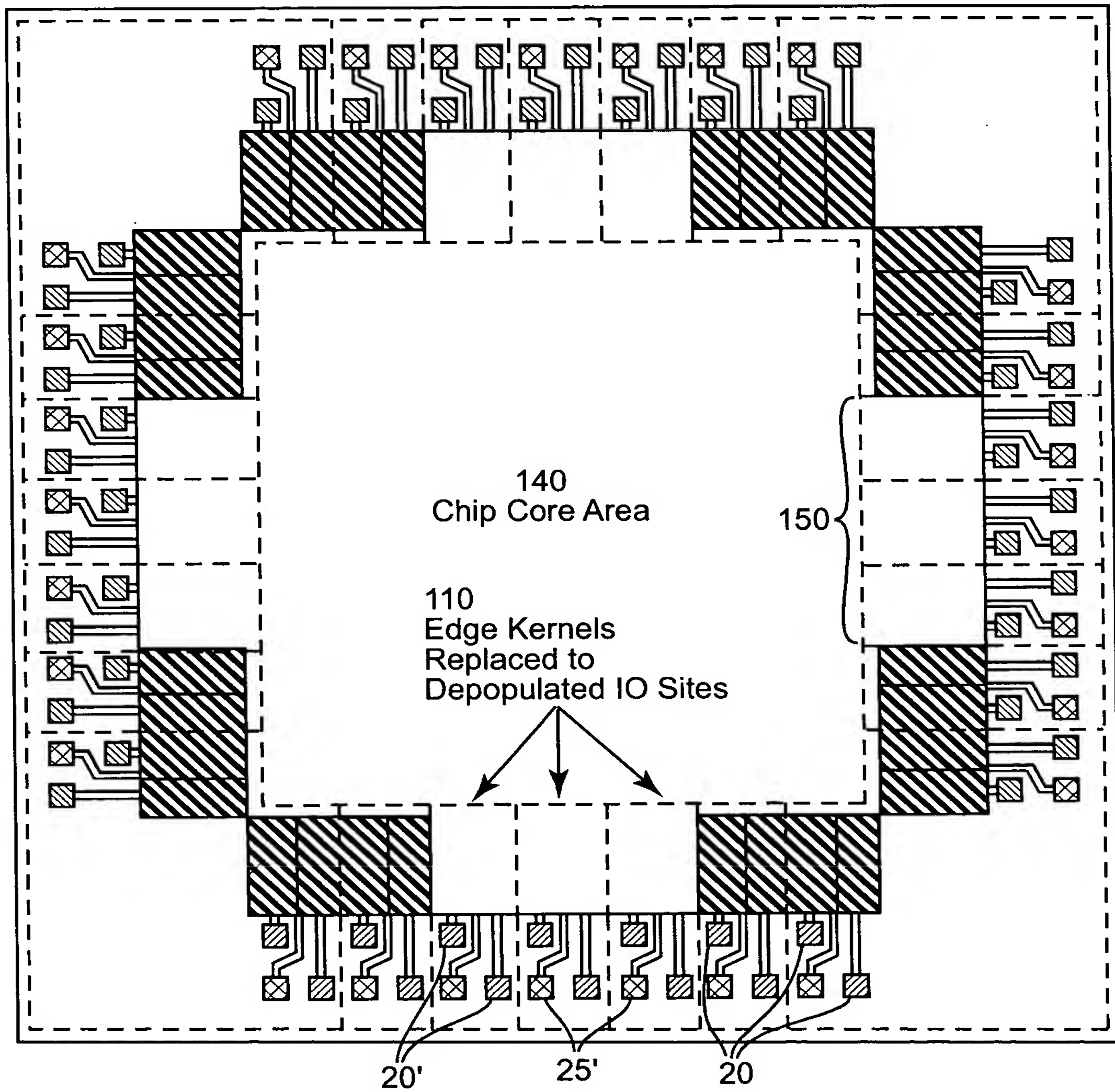
*Figure 1*  
*(RELATED ART)*



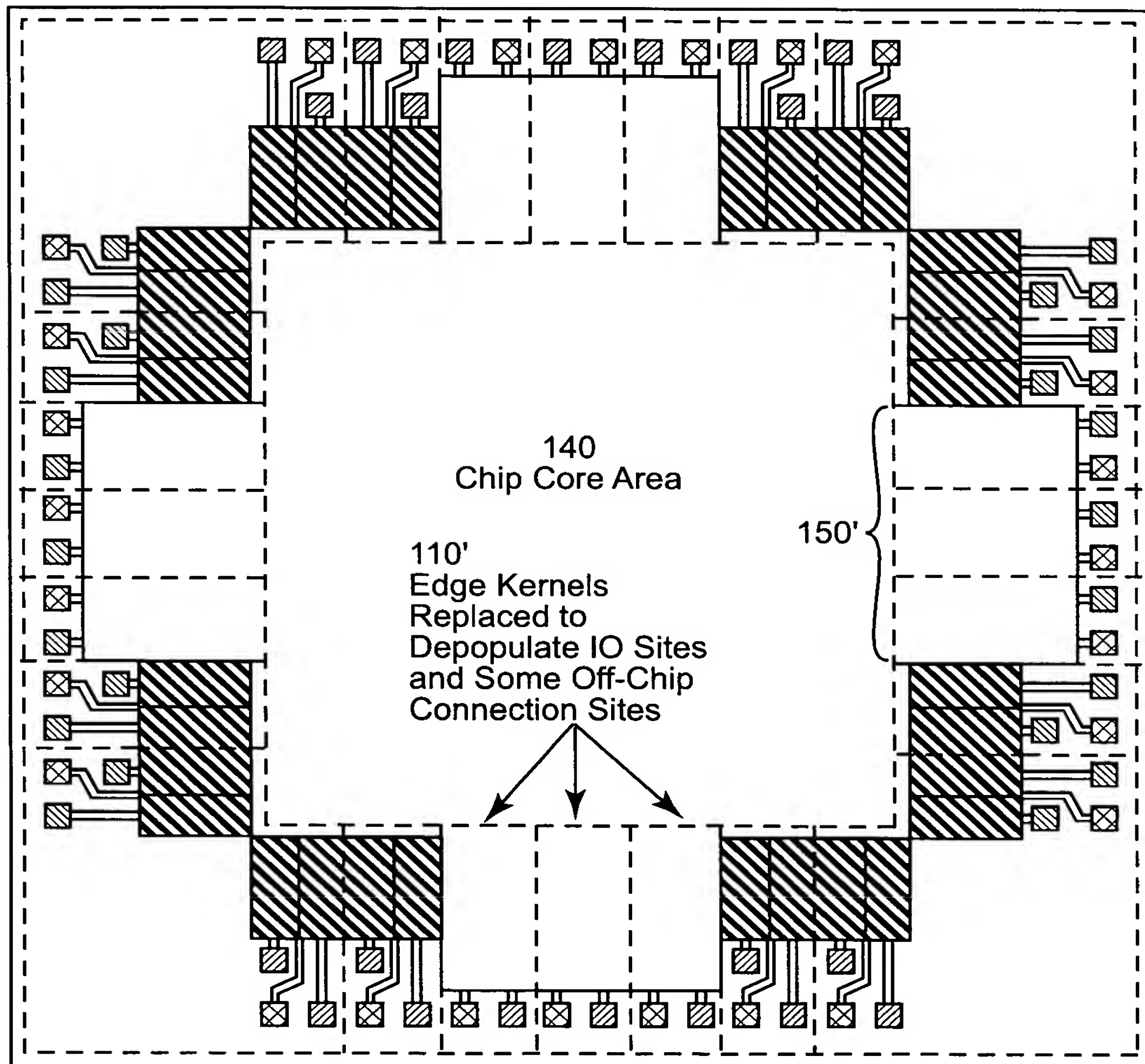
*Figure 2*  
*(RELATED ART)*



*Figure 3*  
*(RELATED ART)*



*Figure 4*



*Figure 5*



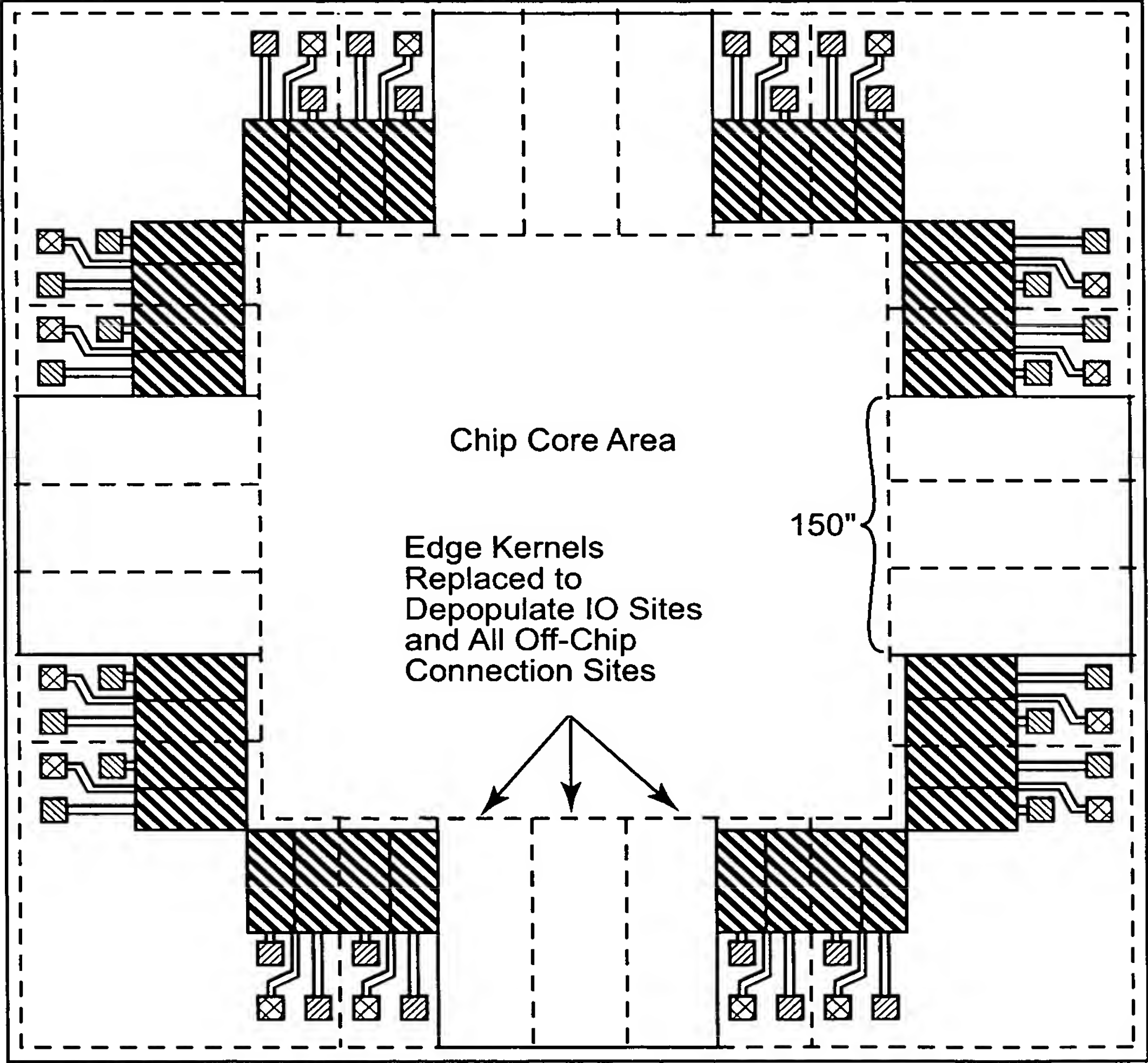
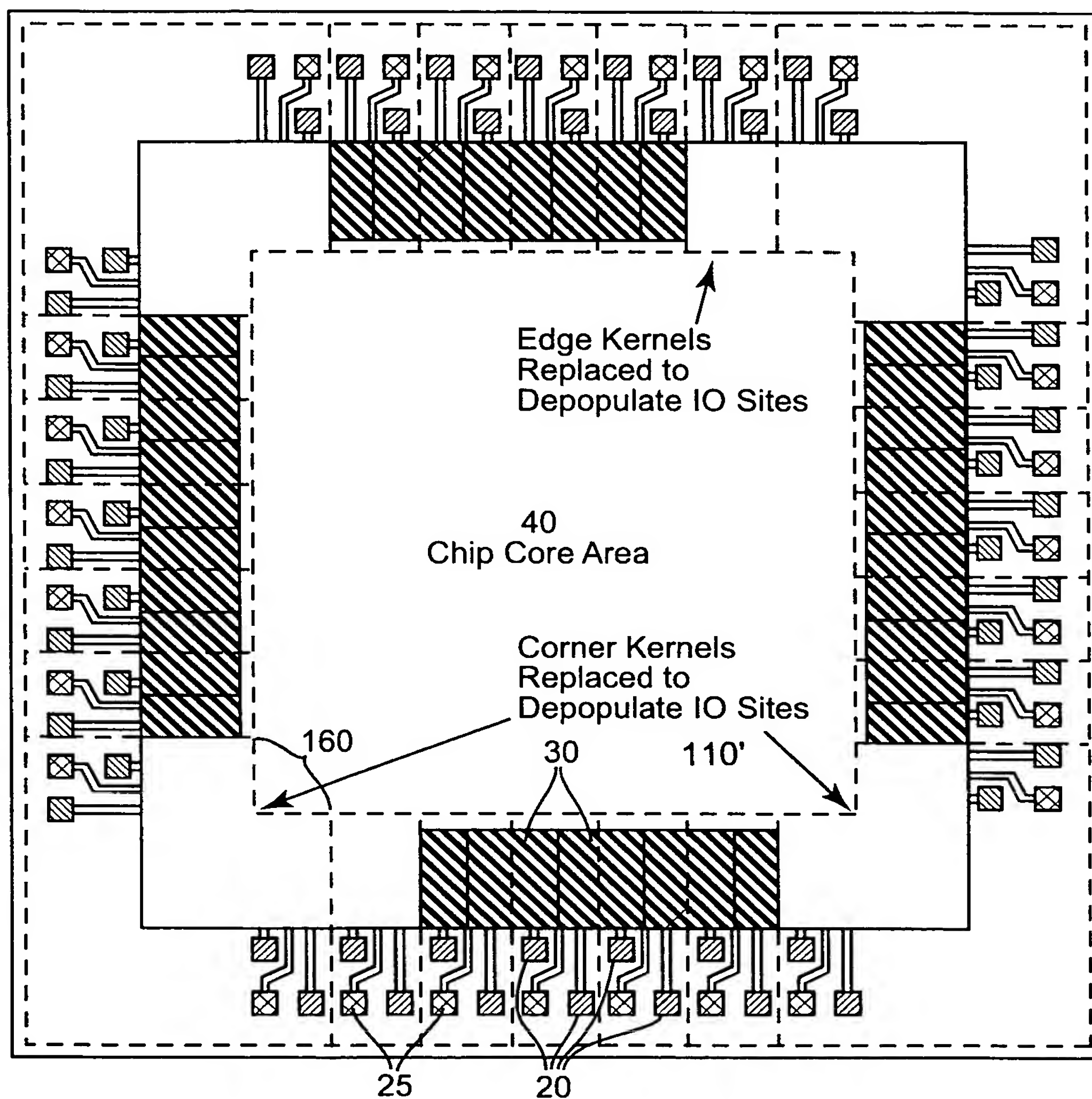
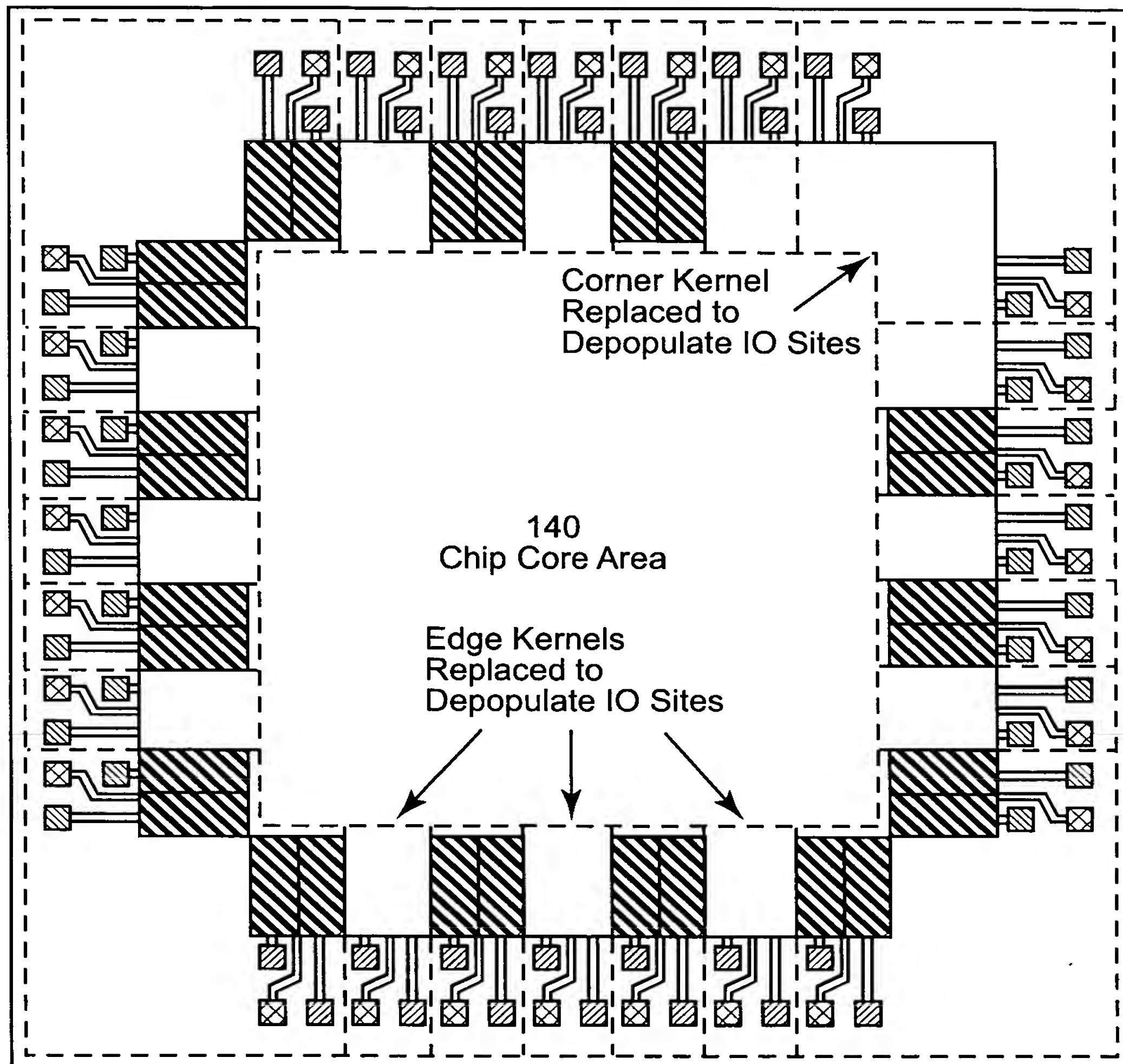


Figure 5A

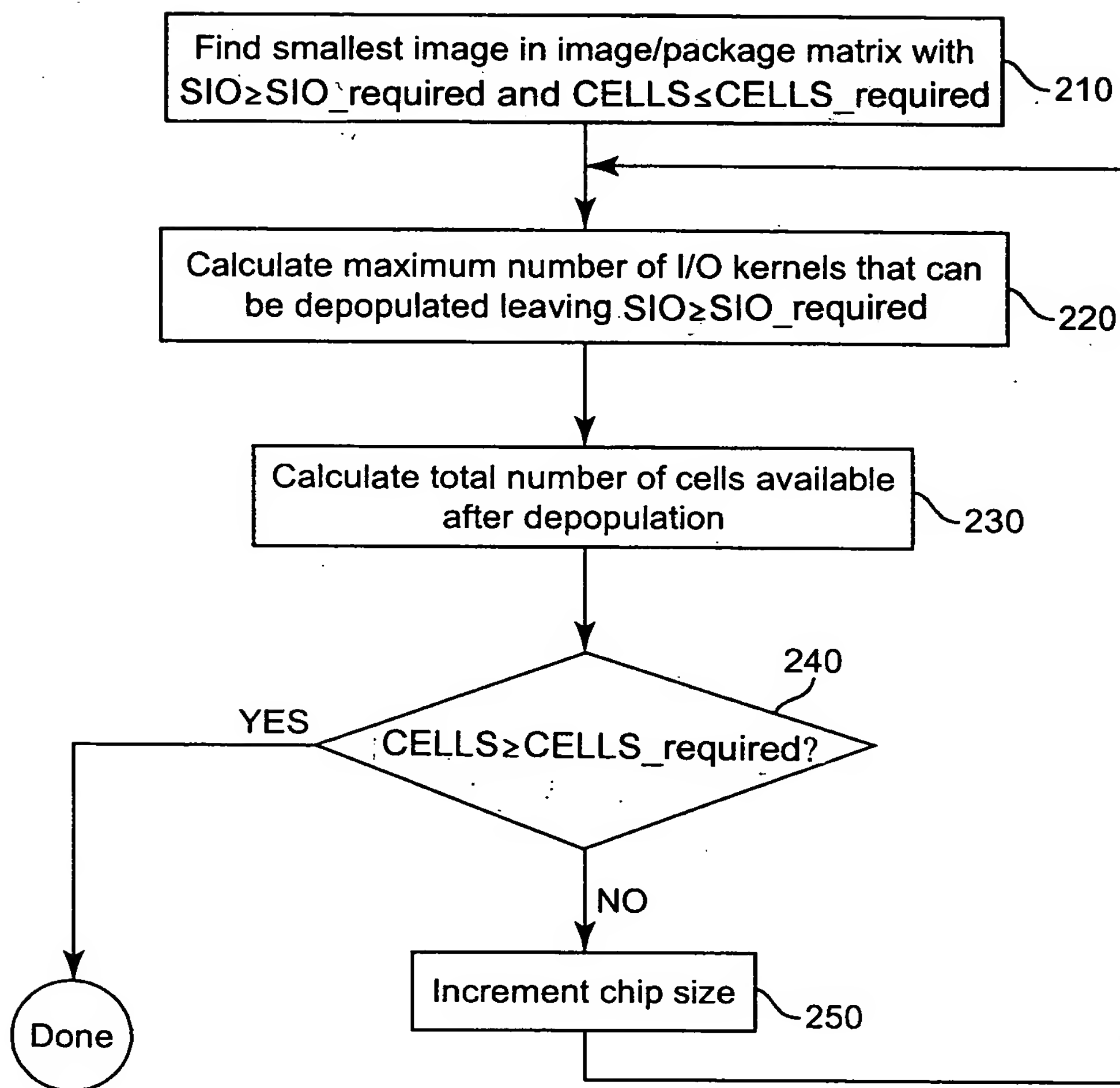


*Figure 6*



*Figure 7*





*Figure 8*

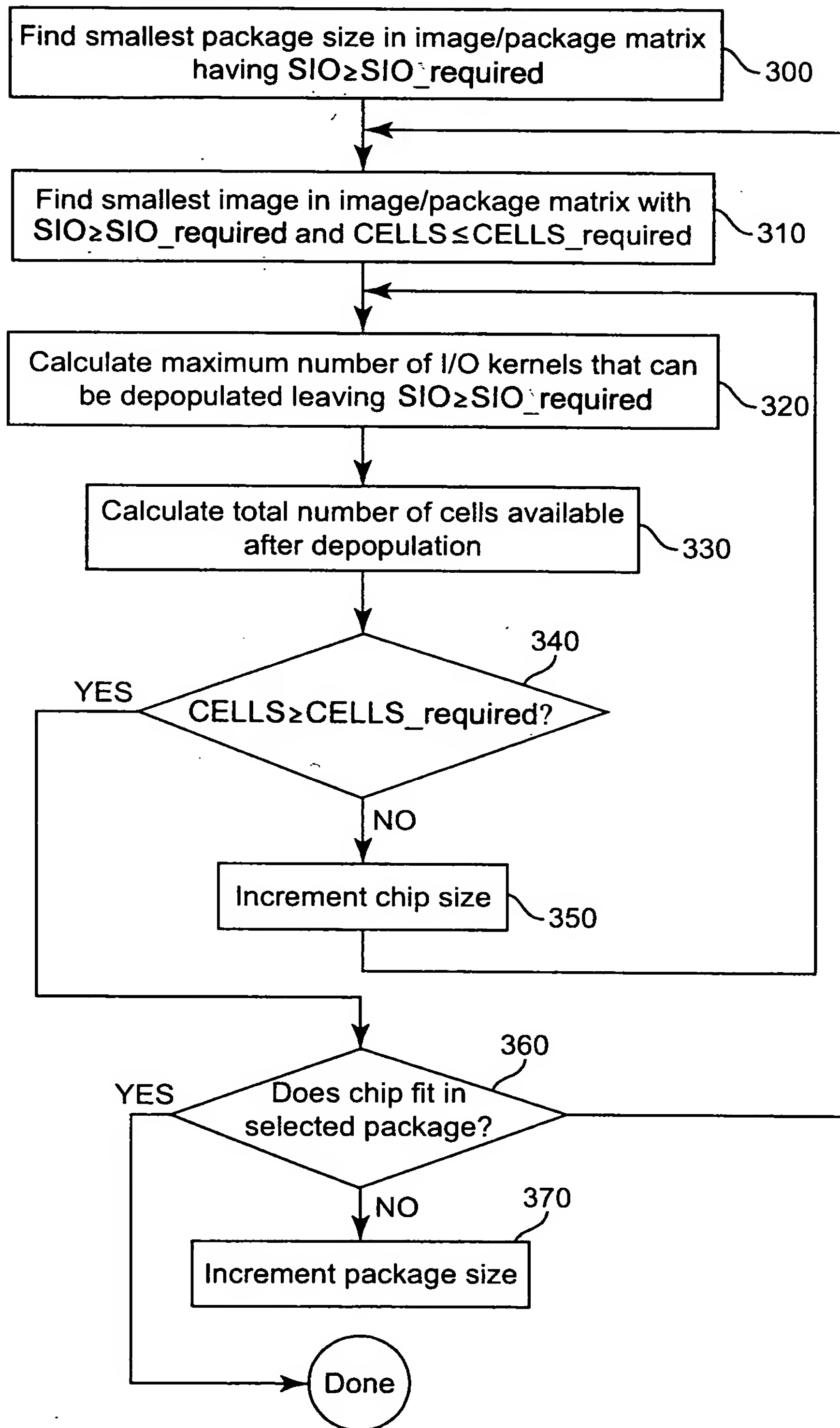


Figure 9

Chip Image	4.85 mm x 4.85 mm	5.58 mm x 5.58 mm	6.30 mm x 6.30 mm
Core Cell Area (dimensions)	3.89 mm x 3.89 mm	4.62 mm x 4.62 mm	5.34 mm x 5.34 mm
Core Cell Area	15.13 mm <sup>2</sup>	21.34 mm <sup>2</sup>	28.62 mm <sup>2</sup>
Total Usable IO cell sites	352	416	480
# of edge kernel (per side)	8	10	12
# of corner kernel (per corner)	1	1	1

Usable IO Sites per Edge Kernel	8
Core Area Recovered by replacing an edge kernel	0.36 mm <sup>2</sup>
Usable IO Sites per Corner Kernel	24
Core Area Recovered by replacing a corner kernel	1.0 mm <sup>2</sup>

Figure 10